REMARKS

Reconsideration of this application is respectfully requested in light of the foregoing amendments and the following remarks.

Claim 60 has been amended solely for purposes of consistency, and thus, not for reasons related to patentability.

Claims 52-62 are now pending in this application. Claims 52 and 59 are the independent claims.

I. The Indefiniteness Rejection

Claims 60 and 61 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite. This rejection is respectfully traversed.

Claim 60 has been amended solely for purposes of consistency, per the Examiner's suggestion.

Thus, reconsideration and withdrawal of this rejection is respectfully requested.

II. The Obviousness Rejection

Claims 52-62 were rejected under 35 U.S.C. § 103(a) as being unpatentable over various combinations of Roy (U.S. Patent No. 6,321,331) in view of Logan (U.S. Patent No. 6,243,857). These rejections are respectfully traversed.

None of the cited references, either alone or in any combination, establish a *prima facie* case of obviousness. "To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to

combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." See MPEP § 2143.

Logan debugs a PLC program "upon interrupt". See col. 4 lines 1-14. Roy requires "a debugging interface for tracing instructions without loss of real time context and event interaction". See col. 2 lines 49-52. By "real time", Roy "means the rate at which a program must execute tin order to process the incoming data rate which may be quite high." See col. 1, lines 24-27. Roy describes real time debugging as helpful for identifying if an "error in program execution is the results of timing errors or other types of errors which only occur when the program is running at real time speed." See col. 1, lines 21-24.

Roy states that "prior art methods of trapping instructions at a given point in time implies that the system must be stopped to allow debugging of firmware. Once the system is stopped, however, real time events and their timing relationships are lost." See col. 2, lines 38-43. Thus, **Roy teaches away** from Logan's "interrupts".

Moreover, one of ordinary skill in the art would not have had a reasonable expectation of success in combining Logan with Roy. Any such combination would render at least Roy inoperable for its intended purpose and/or change the principal of operation of at least Roy. Specifically, attempting to combine Logan with Roy would result in an "interrupt" of the "real time context and event interaction" required by Roy, thus rendering Roy inoperative for its intended purpose. Thus, any attempt to combine Logan with Roy would render at least Roy inoperative or unfit for its intended purpose.

Thus, Roy and/or Logan fail to establish a *prima facie* case of obviousness for claims 52-62. Consequently, reconsideration and withdrawal of these rejections is respectfully requested.

III. Allowable Subject Matter

The following is a statement of reasons for the indication of allowable subject matter:

1. Claims 52-58 recite "debugging a program in real time and while said program is executed ... compiling said section of said program to be debugged in another section of memory ... and jumping to said another section of said memory during execution of said program when an instruction indicated to be debugged is to be executed", which none of the art of record teaches or suggests.
2. Claims 59-62 recite "an apparatus that debugs a program in real time ... another area of memory for storing a compiled section of said program to be debugged ... a branch that causes execution of said program to jump from said original compiled code to said another section of said memory during execution of said program when an instruction indicated to be debugged is to be executed", which none of the art of record teaches or suggests.

AMENDMENT UNDER 37 C.F.R. 1.116

EXPEDITED PROCEDURE

EXAMINING GROUP 2124

PATENT

Serial No. 09/732,570

Attorney Docket No. 1999P07535US04 (1009-064)

CONCLUSION

It is respectfully submitted that, in view of the foregoing amendments and remarks, the application as amended is in clear condition for allowance. Reconsideration, withdrawal of all grounds of rejection, and issuance of a Notice of Allowance are earnestly solicited.

The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. §1.16 or §1.17 to Deposit Account No. 50-2504. The Examiner is invited to contact the undersigned at 434-972-9988 to discuss any matter regarding this application.

Respectfully submitted,

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Date: 13 August 2004

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